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10/091,432	03/07/2002	Shigetaka Asano	1076.1073	8832

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,432	ASANO, SHIGETAKA	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-23* is/are allowed.

6)☒ Claim(s) *1,2 and 4-14* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Remarks/Amendments filed by the applicant on 10/21/2005.

2. Amendment of claim 10, filed by the applicant, is hereby acknowledged. The amendment is considered acceptable and therefore, the rejection of claim 10, under 35 U.S.C. 112, 2nd paragraph has been withdrawn. Additionally, objection of claims 3,14, 15 and 19 is withdrawn based on amendment of the claims by the applicant.

Response to Remarks/Arguments

3. Applicant's remarks/amendments see page 9, filed 10/21/2005, regarding claims 8-14 have been fully considered but are not persuasive.

4. The applicant alleges that Qureshi with reference to claim 14, does not recite "a delay circuit for receiving the analog signal, and delaying the analog signal corresponding to a latency (delay) caused by the first control loop". The examiner respectfully, would like to draw applicant's attention to Qureshi, fig. 2; elements 58, 60, 62 wherein element 58 receives an analog signal from the transmitter (112), the audio interface (58) is connected to a low pass filter (60) establishing a closed loop with the AGC element 62 composed of multiplier 126 and a latch 124. The analog signal r(t) input to the filter as best understood by the examiner implies an inherent delay introduction to incoming analog signal regarded as transmission delay or latency by filters processing the signals (see fig. 2, elements 112, 58, 60, 62; col. 2, lines 30-34; col. 4,

lines 8-14). Based on information disclosure by Qureshi, the examiner firmly believes that Qureshi clearly addresses the claimed limitations recited in claim 14. The claim rejection is, therefore, maintained.

As per applicant's assertion, with reference to limitations of claims 9-13, that Qureshi, Oishi and Gurvich combination does not recite the overcome the claimed limitation in claim 9-13, the examiner respectfully disagrees. When an obviousness determination relies on the combination of two or more references, there must be some suggestion or motivation to combine the references. See In re Rouffet, 149 F. 3d 1350, 1355, 47 USPD 2d 1453, 1456 (Fed. Cir. 1998). The suggestion to combine may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved. See id. at 1357, 47 USPQ 2d at 1458. Moreover, as long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor. See In re Dillon, 919 F .2d 688, 693, 16 USPQ 2d 1897, 1901 (Fed. Cir. 1990) (en banc), cert. Denied, 500 U.S. 904 (1991) and In re Beattie, 974 F .2d 1309, 1312, 24 USPQ 2d 1040, 1042 (Fed. Cir. 1992). Thus, as stated by the examiner, the advantages described by Oishi and Gurvich would have motivated one of ordinary skill in the art to employ capacitor to delay and switch to operate in a synchronous way with the clock signal in the analog signal controller of Qureshi.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 4-7, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Qureshi (USP 4,439,864).

Regarding claims 1 and 6, Qureshi discloses, an analog signal control method comprising:

converting the analog signal to a digital signal (ADC 62) (col. 2, lines 30-37);

performing an arithmetic processing (78) of the digital signal to generate a control signal for controlling the analog signal (col. 2, lines 23-60; col. 4, lines 8-20);

delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal (in synchronism with the clock signal – crystal oscillator 96 generates clock signal which is provided to SPE and MPU 30) (col. 6, lines 15-42); and

controlling the delayed analog signal in accordance with the control signal (col. 3, lines 38-45).

Regarding claim 7, Qureshi discloses an analog signal controller comprises:

an ADC (figs. 2, 3, element 64) for analog-to-digital converting an analog signal to generate a digital signal (col. 2, lines 30-37);

a digital arithmetic circuit (78) connected to the ADC for performing an arithmetic processing of the digital signal to generate a control signal for controlling the analog signal (col. 2, lines 56-66);

a delay circuit for receiving the analog signal, and delaying the analog signal corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal (col. 4, lines 8-20; col. 6, lines 15-20); and

an analog control circuit connected to the digital arithmetic circuit and the delay circuit for controlling the delayed analog input signal in accordance with the control signal (col. 2, lines 56-67; col. 7, lines 3-7).

Regarding claim 14, Qureshi discloses an automatic gain controller comprising:

a first control loop (62) for receiving an analog signal generate a control signal for setting a predetermined gain for use in amplifying the analog signal (col. 3, lines 39-46; col. 4, lines 8-60);

a delay circuit (204) receiving the analog signal, delaying the analog signal corresponding to a control delay(control delay=latency) caused by the first control loop generate a delayed analog signal (col. 4, lines 8-20); and

a GCA connected to the delay circuit and the first control loop for amplifying the delayed analog signal in accordance with a predetermined gain set by the control signal to generate an amplified analog signal (col. 3, lines 39-46; col. 4, lines 8-60).

As per claim 2, Qureshi discloses analog signal control method wherein:

the step of converting includes sampling the analog signal at a predetermined timing to generate a sampling value (abstract; col. 1, lines 21-35);

the step of generating a control signal includes generating the control signal in accordance with the sampling value (col. 1, lines 30-35; col. 2, lines 38-44); and

the step of delaying includes delaying the analog signal to control the analog signal in accordance with the control signal, the analog signal having a sampling value corresponding the predetermined sampling timing (the processor compares the average and the desired (predetermined) levels) (col. 6, lines 15-21).

Regarding claims 4 and 5, Qureshi discloses an analog signal control method wherein:

the step of converting includes sampling the analog signal (A/D 62 provides inherent sampling) at a predetermined timing to generate a sampling value (abstract; col. 1, lines 21-35);

the step generating a control signal includes generating the control signal in accordance with the sampling value (col. 1, lines 30-35; col. 2, lines 15-44); and

the step of delaying includes delaying the analog signal by the latency to control the analog signal in accordance with the control signal, the analog signal having a sampling value produced by sampling the analog signal at a timing previous to the predetermined sampling timing (col. 6, lines 50-59).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (USP 4,439,864) in view of Oishi et al (US Patent 6,563,859).

Regarding claim 8, Qureshi discloses an analog signal controller wherein: the analog signal controller operates in accordance with a clock signal (col. 1, lines 30-35; col. 2, lines 15-44). Qureshi however is silent regarding "the delay circuit includes a pair of switches which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the pair of switches". Oishi in a similar field of endeavor discloses a plurality of delay switches (fig. 12501-1 to 501-N), which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the plurality of switches (col. 11, lines 18-34). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use delay switches to delay analog signals (sampling period of the A/D converters) in synchronism with the clock signal as taught by Oishi in the circuit of Qureshi because it can provide equalization in frequency shift of the received signal to be extracted.

9. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (USP 4,439,864) in view of Gurvich (US Patent 6,897,724).

Regarding claims 12 and 13, Qureshi discloses all of the claim limitations but is silent regarding a delay circuit includes a capacitor having a capacitance (variable) value for delaying the analog signal corresponding to a latency (delay, error). Gurvich in a similar field of endeavor shows a system wherein capacitors are used in the delay circuit for delaying the signal, shows the capacitor could be a variable capacitor such as a varactor (variable capacitor) (col. 5, lines 25-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to use fixed or variable capacitors at the switch nodes as taught by Gurvich in the circuit of Qureshi because it can lend to proper group delay adjustments with the transmission of signal in the transmission line.

10. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (US Patent 4,439,864) in view of Oishi (US Patent 6,563,859) as applied to claim 8 above, and further in view of Gurvich (US Patent 6,897,724).

Regarding claim 9 Qureshi in combination with Oishi discloses all of the claim limitations, except delay circuit includes a capacitor connected to a node between pair of switches and a ground. Gurvich in a similar field of endeavor discloses a system for adjusting group delay wherein delay circuit includes a capacitor (or a variable capacitor 501, 602) connected to a node (303) between pair of switches and a ground (figs. 3-6, elements 302, 403, 501) (col. 5, lines 26-37). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use fixed or variable capacitors at the switch nodes as taught by Gurvich in the circuit of Qureshi and Oishi because it can lend to proper group delay adjustments with the transmission of signal in the transmission line.

Regarding claim 10, Qureshi in combination with Oishi discloses all of the claim limitations, except the delay circuit further includes a selector circuit for selecting the plurality of delay stages in accordance with the sampling value of the analog signal. Gurvich in a similar field of endeavor discloses the delay circuit further includes a selector circuit for selecting the plurality of delay stages in accordance with the sampling value of the analog signal (col. 7, lines 50-67; col. 8, lines 1-2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use selector circuit for selecting a plurality of delay stages as

taught by Gurvich in the circuit of Qureshi and Oishi because it can selectively mitigate delays with the transmission of signal in the transmission line.

Regarding claim 11, Qureshi in combination with Oishi discloses all of the claim limitations except a capacitor connected between a node and a ground. Gurvich in a similar field of endeavor further discloses a capacitor (302) connected between a node and a ground (fig. 3; col. 5, lines 26-30). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a capacitor at switch nodes as taught by Gurvich in the circuit of Qureshi and Oishi because it can achieve adequate group delay adjustments and suitable impedance matching of delay stages.

Allowable Subject Matter

11. Claims 15-18, 19-23 allowed.

12. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEAN B. CORRIELUS
PRIMARY EXAMINER
12-9-05

QG.
December 8, 2005.